Clocks and Triggers

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Obtaining 2's complement

2's complement: $2^N - b$

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$$
\begin{array}{r r r r r r}
 & 1 & 0 & 0 & 0 & 0 \\
- & & b_3 & b_2 & b_1 & b_0 \\
\hline
 & & c_3 & c_2 & c_1 & c_0
\end{array}
$$

← 2's complement (complementary code)

Obtaining 2's complement

2's complement: $2^N - b$

$$\begin{array}{cccccc} & 1 & 0 & 0 & 0 & 0 \\ - & & b_3 & b_2 & b_1 & b_0 \\ \hline & & c_3 & c_2 & c_1 & c_0 \end{array}$$

$\leftarrow$ 2's complement (complementary code)

$$2^N - b = (2^N - 1) - b + 1$$

Obtaining 2's complement

2's complement: $2^N - b$

$$\begin{array}{cccccc} & 1 & 0 & 0 & 0 & 0 \\ - & & b_3 & b_2 & b_1 & b_0 \\ \hline & & c_3 & c_2 & c_1 & c_0 \end{array}$$

← 2's complement (complementary code)

$$2^N - b = (2^N - 1) - b + 1$$

$$1\,0000_2 = 1111_2 + 1$$

Obtaining 2's complement

2's complement: $2^N - b$

$$\begin{array}{rccccc} & 1 & 0 & 0 & 0 & 0 \\ - & & b_3 & b_2 & b_1 & b_0 \\ \hline & & c_3 & c_2 & c_1 & c_0 \end{array} \leftarrow \text{2's complement (complementary code)}$$

$$2^N - b = (2^N - 1) - b + 1$$

$$1\,0000_2 = 1111_2 + 1$$

$$\begin{array}{rccccc} & 0 & 1 & 1 & 1 & 1 \\ - & & b_3 & b_2 & b_1 & b_0 \\ \hline \end{array} \leftarrow (2^N - 1)$$

$$\begin{array}{rccccc} & & \overline{b_3} & \overline{b_2} & \overline{b_1} & \overline{b_0} \\ + & & & & & 1 \\ \hline & & c_3 & c_2 & c_1 & c_0 \end{array}$$

$\overline{b_3}\,\overline{b_2}\,\overline{b_1}\,\overline{b_0}$ ← 1's complement (inverse code)

$c_3\,c_2\,c_1\,c_0$ ← 2's complement

2's complement example

$$10_2 - 11_2 = ???$$

Find 2's complement of 11_2:

$$\begin{array}{cccccc} & 0 & 1 & 1 & 1 & 1 \\ - & & 0 & 0 & 1 & 1 \\ \hline & & \overline{0} & \overline{0} & \overline{1} & \overline{1} \\ & & 1 & 1 & 0 & 0 \\ + & & & & & 1 \\ \hline & & 1 & 1 & 0 & 1 \end{array}$$

$\leftarrow (2^N - 1)$

$\leftarrow$ 1's complement

$\leftarrow$ 2's complement

$$10_2 - 11_2 = 0010_2 + 1101_2 = 1111_2 = -1_2$$

Converting 2's complement to decimal

Dec.	2's Compl.	Dec.	2's Compl.
7	0111	-1	1111
6	0110	-2	1110
5	0101	-3	1101
4	0100	-4	1100
3	0011	-5	1011
2	0010	-6	1010
1	0001	-7	1001
0	0000	-8	1000

Converting 2's complement to decimal

Dec.	2's Compl.	Dec.	2's Compl.
7	0111	-1	**1**111
6	0110	-2	**1**110
5	0101	-3	**1**101
4	0100	-4	**1**100
3	0011	-5	**1**011
2	0010	-6	**1**010
1	0001	-7	**1**001
0	0000	-8	**1**000

The most significant bit (MSB) of a negative number is **1**

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The most significant bit (MSB) of a negative number is **1**
The smallest representable negative number has absolute value *larger* than the larger representable positive.

Converting 2's complement to decimal

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3	0011	-5	1011
2	0010	-6	1010
1	0001	-7	1001
0	0000	**-8**	**1000**

$$1011_2 = 1000_2 + 0011_2 = -2^3 + 11_2$$

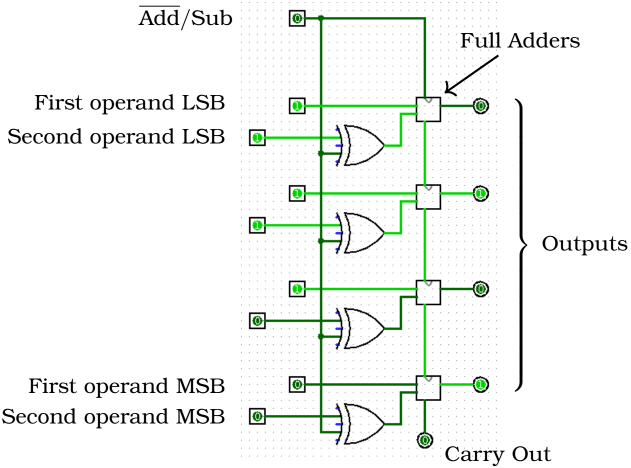
$$= \overset{-2^3}{1}\ \overset{2^2}{0}\ \overset{2^1}{1}\ \overset{2^0}{1}$$

$$= -2^3 + 2^1 + 2^0 = -8_{10} + 2_{10} + 1_{10}$$

$$= -5_{10}$$

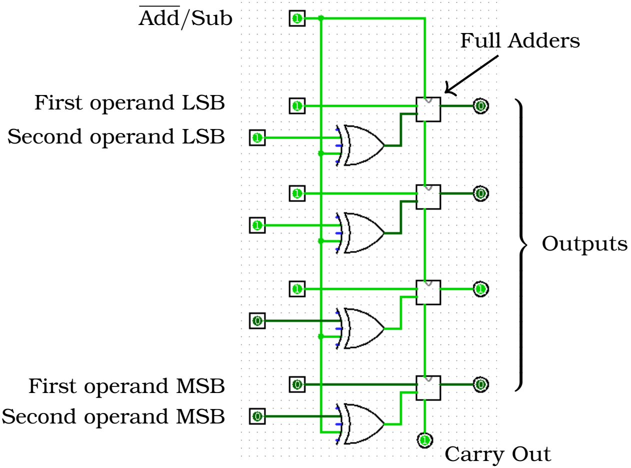
Adder/Subtractor ALU

$$7_{10} + 3_{10} = 0111_2 + 0011_2 = 1010_2 = 10_{10}$$



Adder/Subtractor ALU

$$7_{10} - 3_{10} = 0111_2 - 0011_2 = 0111_2 + 1101_2 = 1\ 0100_2 = 4_{10}$$



Other representations of negative numbers

Signed magnitude:

$$6_{10} = 0110_2; \quad -6_{10} = 1110_2$$

Complement arithmetic:

$$a + (-b) = a + \underbrace{\underbrace{((2^N - 1) - b)}_{\text{one's complement}} + 1}_{\text{2's complement}} - 2^N$$

Excess K (biased) representation:

$$\begin{aligned} K &= \quad 2^{N-1} && \text{(as a rule, but other values are possible)} \\ b &\leftrightarrow \quad K + b = 2^{N-1} + b \\ -b &\leftrightarrow K + (-b) = 2^{N-1} + (-b) \end{aligned}$$

Other representations of negative numbers

Number	Unsigned	2's Compl.	1's Compl.	Sign-Magn.	Exess [1] K
7	111	-	-	-	-
6	110	-	-	-	-
5	101	-	-	-	-
4	100	-	-	-	-
3	011	011	011	011	111
2	010	010	010	010	110
1	001	001	001	001	101
0	000	000	000	000	100
-0	-	-	111	100	-
-1	-	111	110	101	011
-2	-	110	101	110	010
-3	-	101	100	111	001
-4	-	100	-	-	000

See also:
Murdocca et al. 1999, chapt. 2;
Walker 1996, "Minus Zero"

[1] $K = 4 = 2^{N-1}$, $N = 3$

CMOS Oscillators

Fairchild Semiconductor
Application Note 118
October 1974

FAIRCHILD SEMICONDUCTOR TM

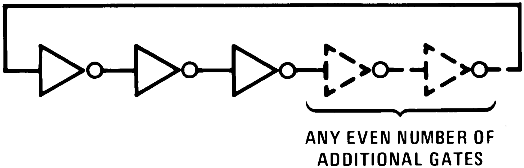


FIGURE 1. Odd Number of Inverters Will Always Oscillate

(Fairchild Semiconductor 1974)

Oscillators

CMOS Oscillators

Fairchild Semiconductor
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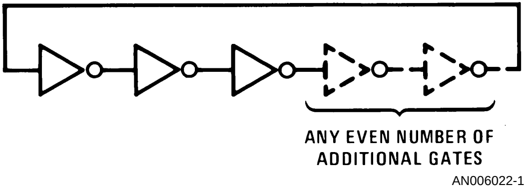
FAIRCHILD SEMICONDUCTOR™

"It then becomes obvious that a "1" chases itself around the ring and the network oscillates." :)



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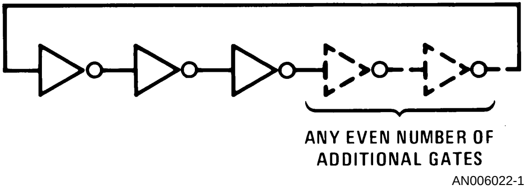
(Fairchild Semiconductor 1974)



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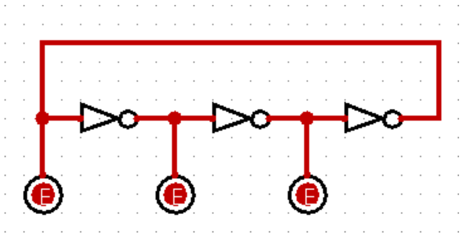
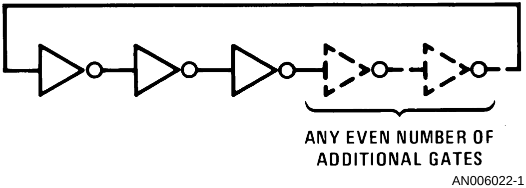


Ring oscillator



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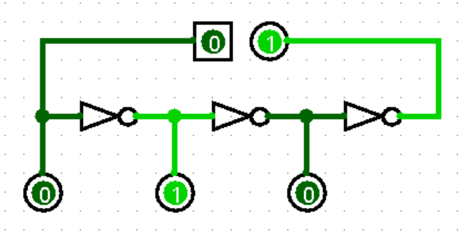
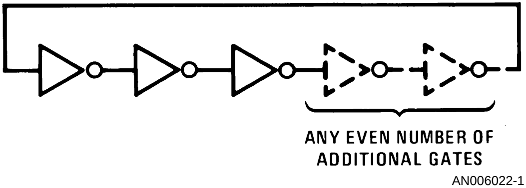


Ring oscillator



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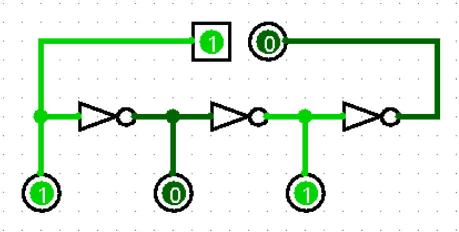
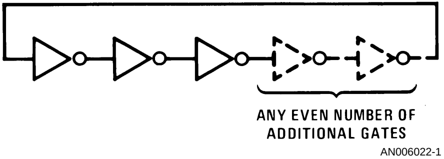


Clock oscillator



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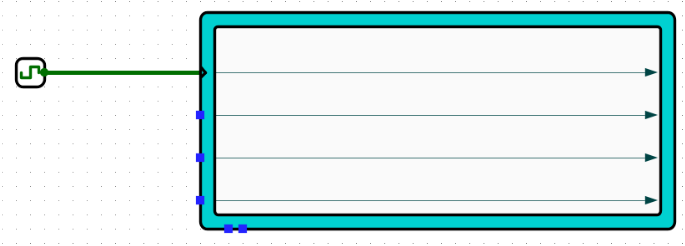
Will Always Oscillate**



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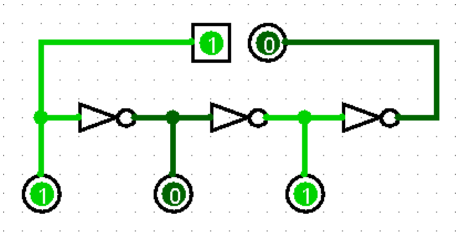
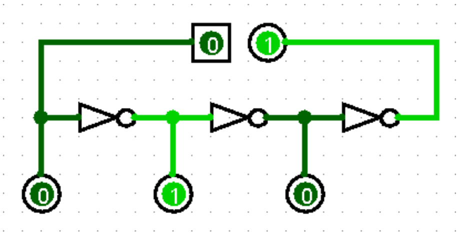
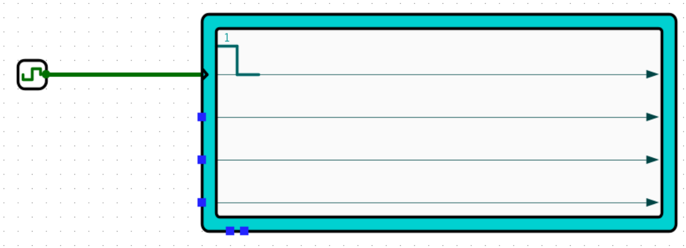


Clock oscillator





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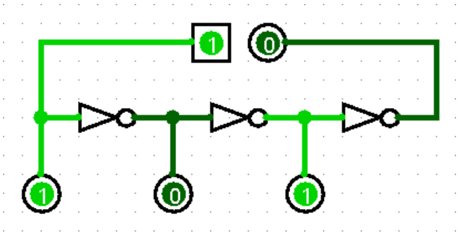

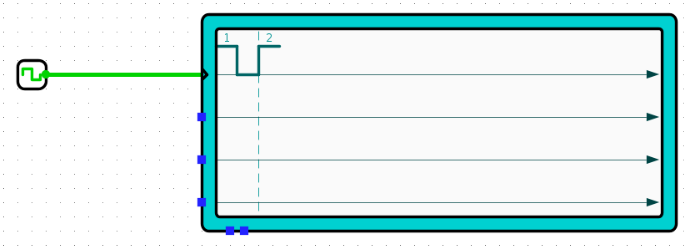

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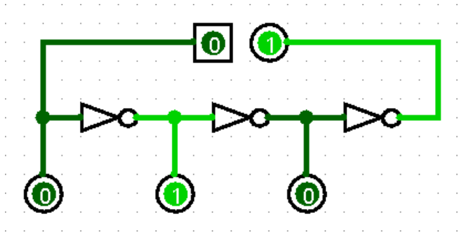

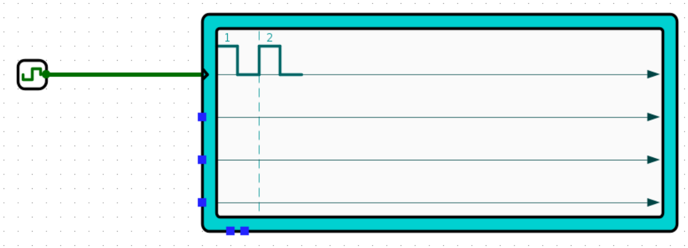

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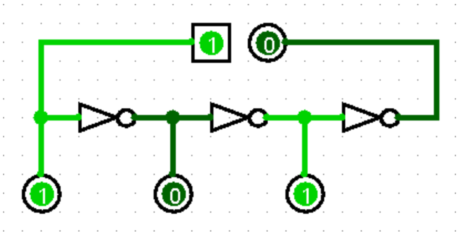

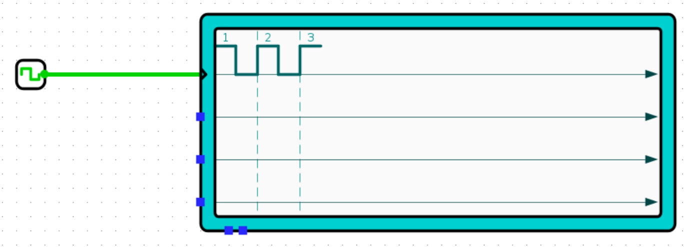

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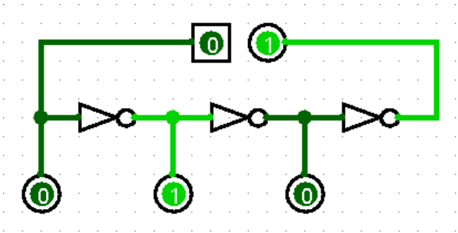

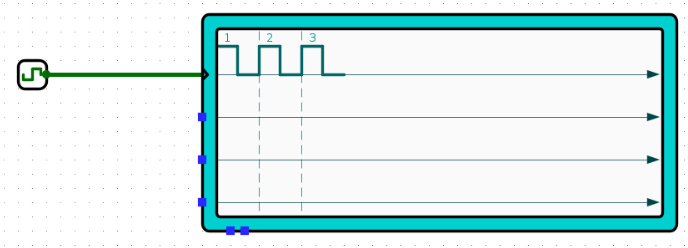

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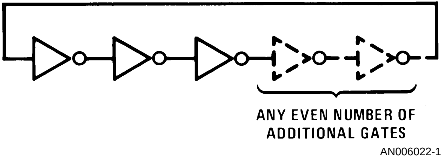

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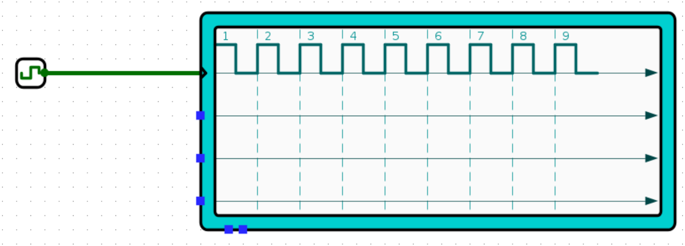
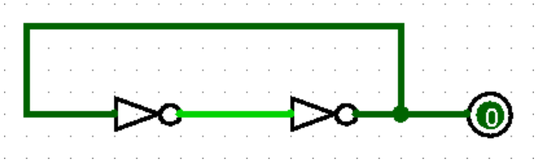


Even number of inverters



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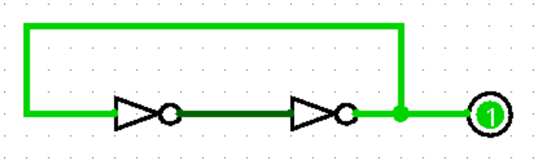

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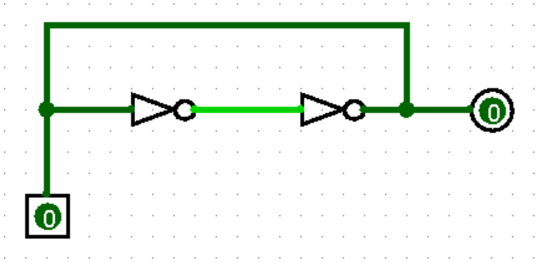

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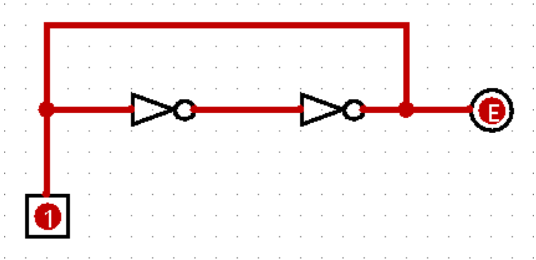
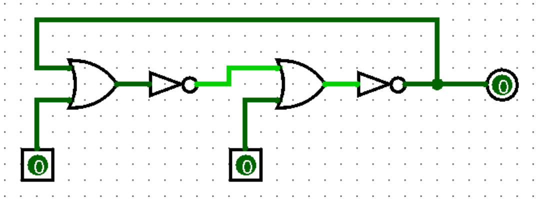


Even number of inverters

Setting state



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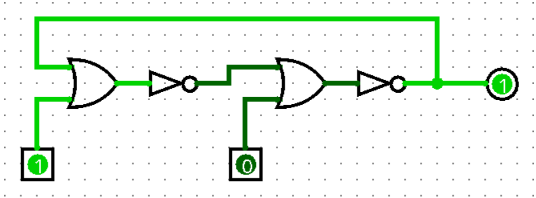

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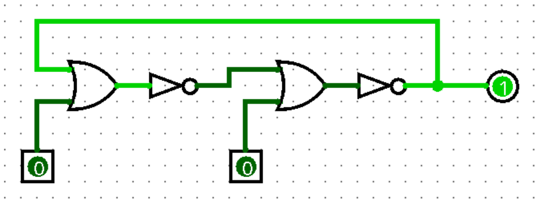

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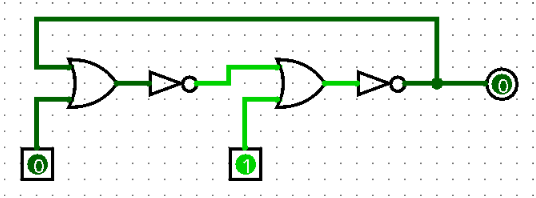

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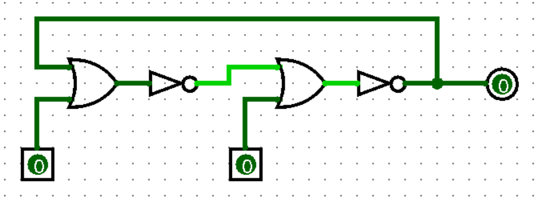
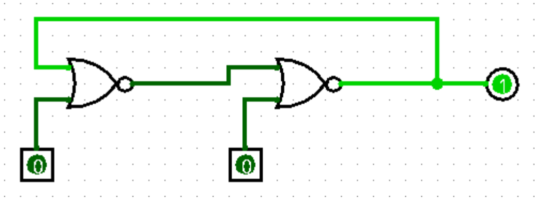


RS trigger from NOR gates



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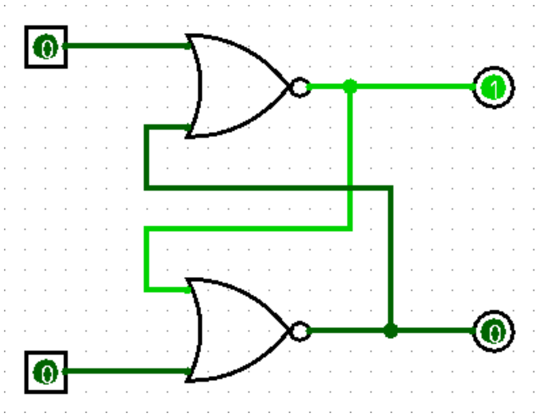
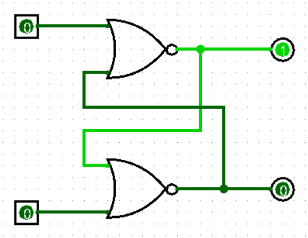
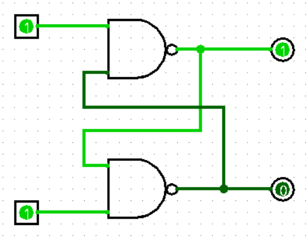


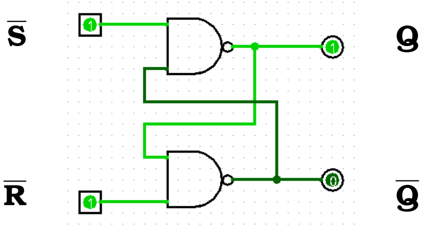
RS trigger from NOR and NAND gates





RS Trigger

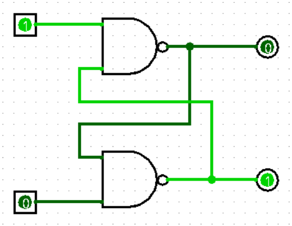
S	**R**	$\overline{\textbf{S}}$	$\overline{\textbf{R}}$	**Q**	
0	0	1	1	Q	←
0	1	1	0	0	
1	0	0	1	1	
1	1	0	0	X	



RS Trigger

S	**R**	$\overline{\textbf{S}}$	$\overline{\textbf{R}}$	**Q**	
0	0	1	1	Q	
0	1	1	0	0	←
1	0	0	1	1	
1	1	0	0	X	

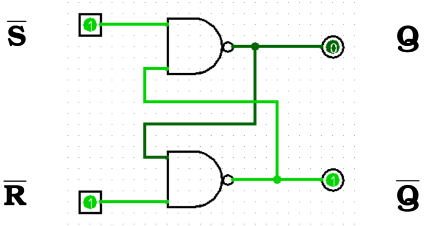
$\overline{\textbf{S}}$ **Q**



$\overline{\textbf{R}}$ $\overline{\textbf{Q}}$

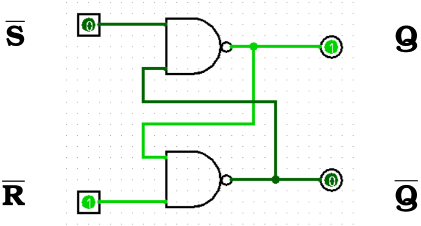
RS Trigger

S	R	$\overline{S}$	$\overline{R}$	Q	
0	0	1	1	Q	←
0	1	1	0	0	
1	0	0	1	1	
1	1	0	0	X	



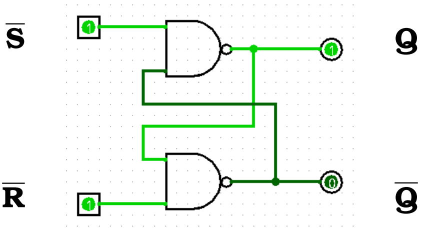
RS Trigger

S	R	$\overline{S}$	$\overline{R}$	Q	
0	0	1	1	Q	
0	1	1	0	0	
1	0	0	1	1	←
1	1	0	0	X	

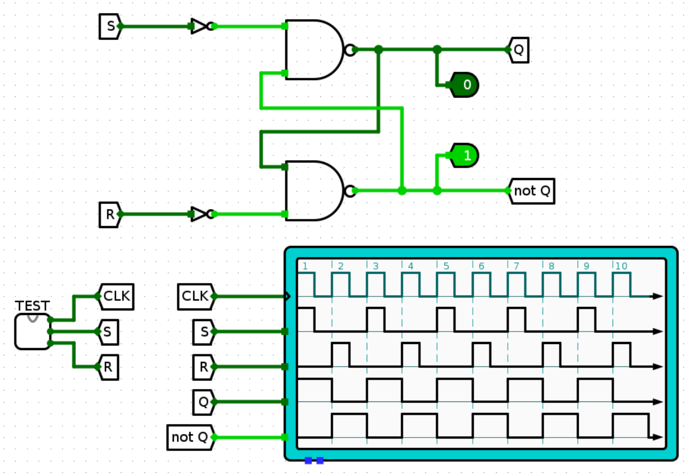


RS Trigger

S	**R**	$\overline{\mathbf{S}}$	$\overline{\mathbf{R}}$	**Q**	
0	0	1	1	Q	←
0	1	1	0	0	
1	0	0	1	1	
1	1	0	0	X	



RS Trigger time traces



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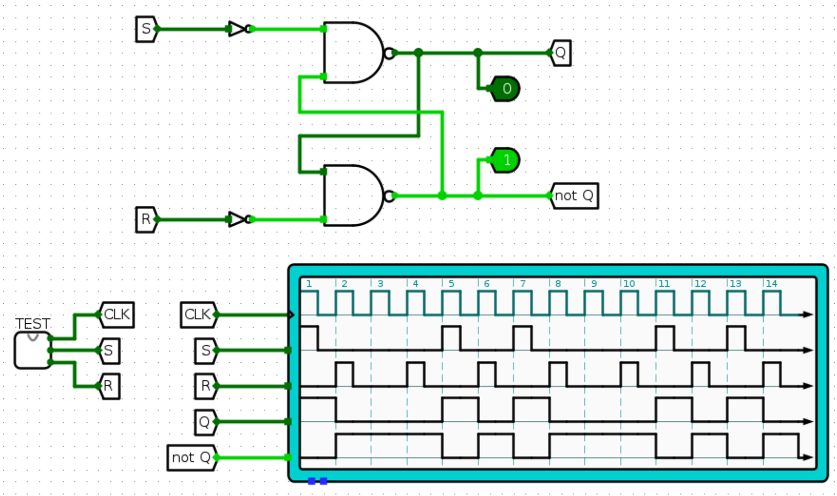
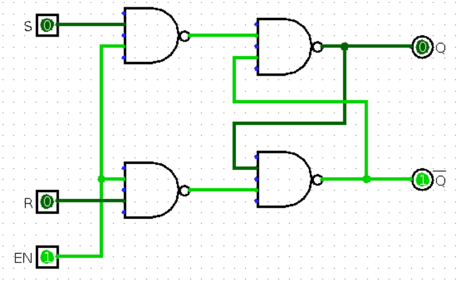
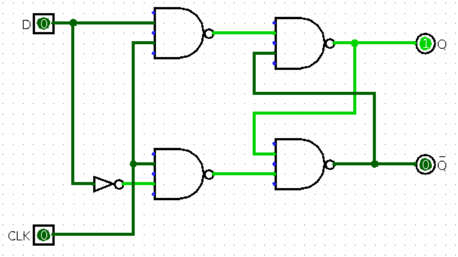


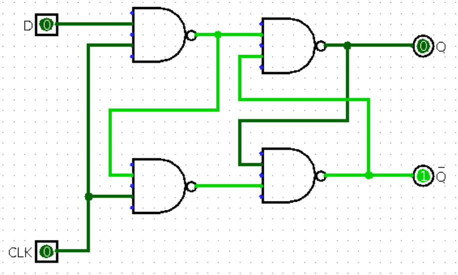
Gated RS Trigger



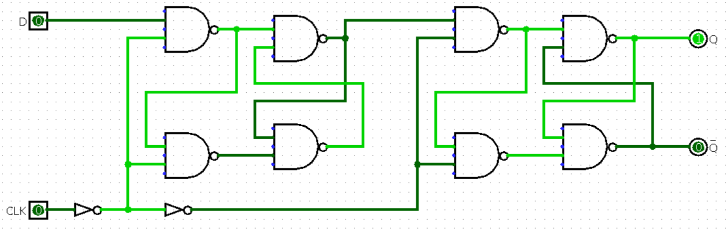
D Latch

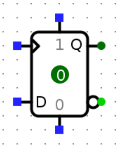


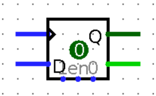
D Latch



Edge-triggered D-flip-flop







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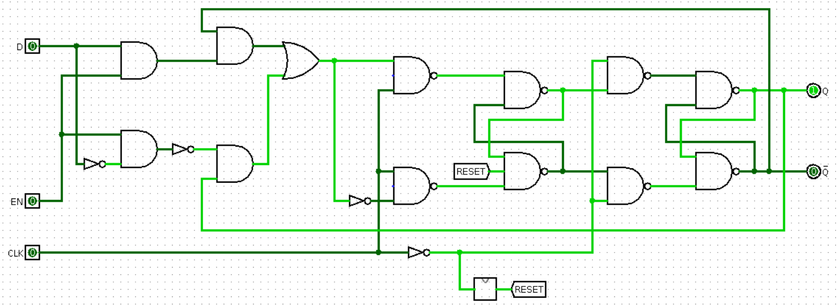
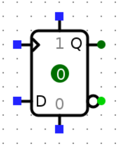
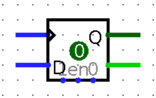
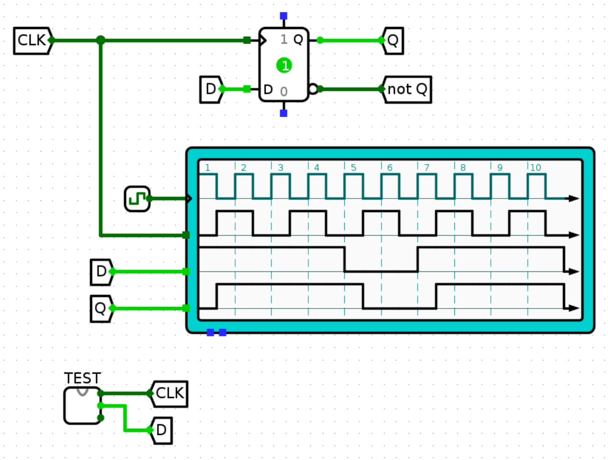


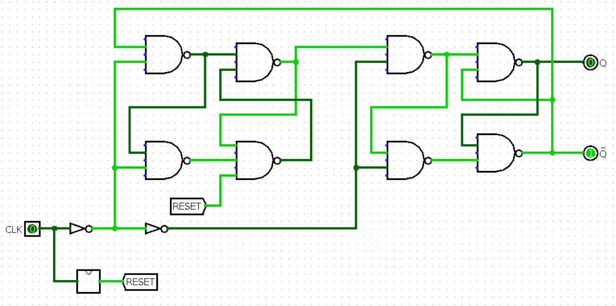


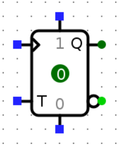


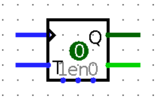
Operation of a D-flip-flop



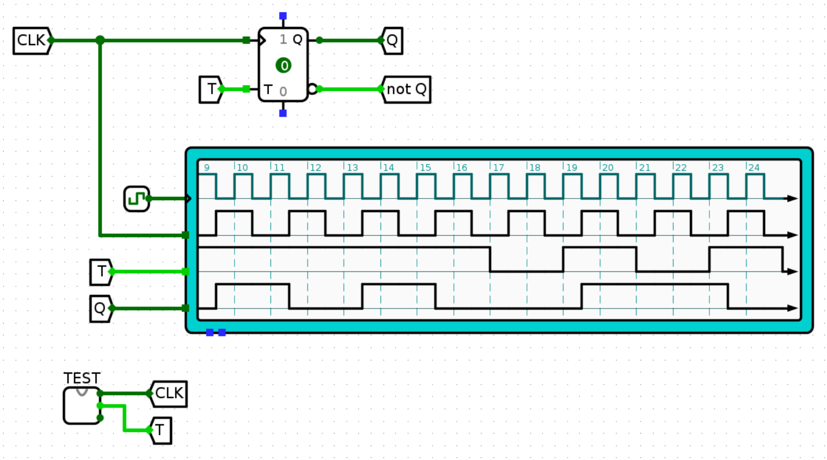
T flip-flop



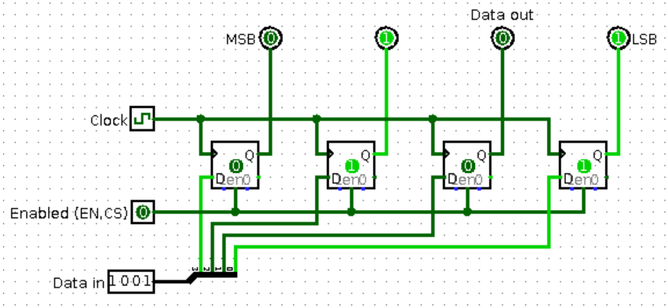




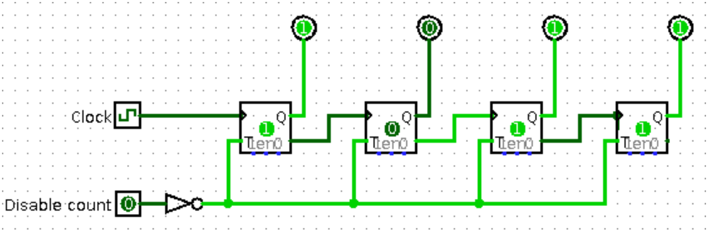
Operation of a T-flip-flop



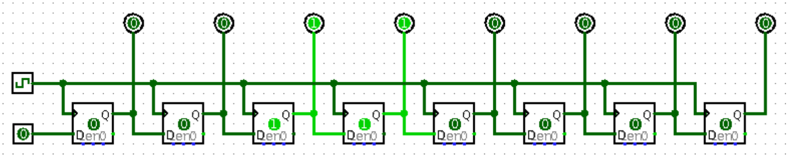
Registers



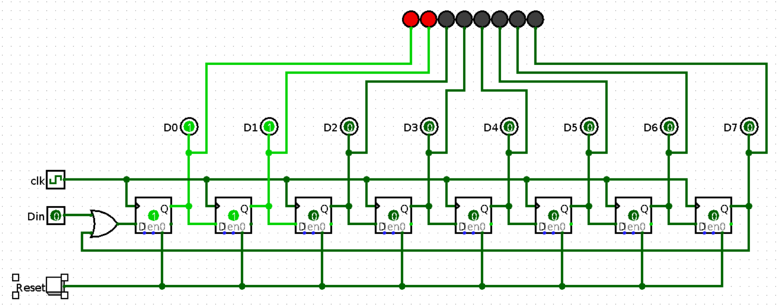
Counters

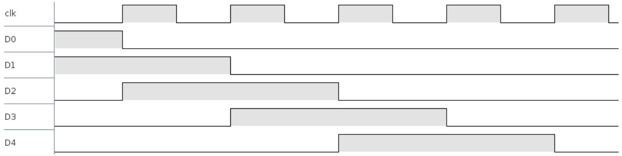


Shift registers



Circular shift registers





Take home messages

- Negative integers are represented in 2's complement in modern computers, but other methods exist and are also used.
- Modern computers are synchronous – they use clock generators to drive their computations
- Feedback is essential to build clocks and memory cells
- From the fundamental RS trigger, gated latches and edge triggered flip-flops (D-, T-flip-flops) are built.
- From D- and T-flip-flops we can further build essential computer components: registers and counters.

References

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